WHAT IS CLAIMED IS:

1. A sampling device, comprising:

a first delay circuit and a second delay circuit in a parallel configuration, the first delay circuit and the second delay circuit responsive to a clock signal;

control circuitry responsive to an output of the first delay circuit and the clock signal, the control circuitry to adjust a delay amount of the first delay circuit based on a difference between the output of the first delay circuit and the clock signal, the control circuitry further responsive to an output of the second delay circuit, the control circuitry further to adjust a delay amount of the second delay circuit based on a difference between the output of the second delay circuit and the clock signal.

2. The device of claim 1, further including data sampling circuitry, the data sampling circuitry responsive to a data signal synchronized with the clock signal.

3. The device of claim 2, wherein the data sampling circuitry is further responsive to a sampling output of the first delay circuit.

4. The device of claim 2, wherein the data sampling circuitry is further responsive to a sampling output of the second delay circuit.

5. The device of claim 1, wherein the first delay circuit includes a first delay element responsive to the clock signal and a second delay element responsive to an output of the first delay element.

6. The device of claim 5, further including data sampling circuitry responsive to a sampling output of the first delay element.

7. The device of claim 1, wherein the second delay circuit includes a first inverting delay element responsive to the clock signal and a second inverting delay element responsive to an output of the first inverting delay element.

8. The device of claim 1, wherein the control circuitry includes a comparator responsive to the output of the first delay circuit and responsive to the clock signal, and wherein the control circuitry further includes a controller responsive to an output of the comparator, the controller to adjust the

delay amount of the first delay circuit based on the output of the comparator.

9. The device of claim 8, wherein the comparator comprises an inverting phase detector.

10. The device of claim 9, wherein the inverting phase detector comprises a phase difference circuit and a sense amplifier.

11. The device of claim 10, wherein the inverting phase detector further comprises a latch.

12. The device of claim 9, wherein the inverting phase detector comprises a flip flop.

13. The device of claim 8, wherein the control circuitry further includes a different comparator responsive to the output of the second delay circuit and responsive to the clock signal, and wherein the control circuitry further includes a different controller responsive to an output of the different comparator, the different controller to adjust the delay amount of the second delay circuit based on the output of the different comparator.

14. The device of claim 1, wherein the device is configured to sample a data signal synchronized with the clock signal according to a double data rate (DDR) protocol.

15. A method of sampling data, comprising:

receiving a clock signal synchronized with a data signal;

generating a first sampling signal based on the clock signal, the first sampling signal delayed by a first delay with respect to the clock signal;

generating a second sampling signal based on the clock signal, the second sampling signal delayed by a second delay with respect to the clock signal, the second delay different than the first delay;

sampling the data signal based on the first sampling signal; and

sampling the data signal based on the second sampling signal.

16. The method of claim 15, further comprising generating a first locking signal delayed by twice the first delay with respect to the clock signal.

17. The method of claim 16, further comprising comparing the first locking signal to the clock signal.

18. The method of claim 17, further comprising modifying the first delay based on the comparing.

19. The method of claim 15, further comprising generating a second locking signal delayed by twice the second delay with respect to the clock signal.

20. The method of claim 19, further comprising comparing the second locking signal to the clock signal.

21. The method of claim 19, further comprising modifying the second delay based on the comparing.

22. The method of claim 15, wherein sampling the data signal based on the first sampling signal comprises sampling the data signal at a midpoint between a first edge and a second edge of the clock signal, wherein the second edge is the next successive edge of the clock signal after the first edge.

23. The method of claim 22, wherein sampling the data signal based on the second sampling signal comprises sampling the data signal at a midpoint between the second edge of the clock signal and a third edge of the clock signal, wherein the third edge is the next successive edge of the clock signal after the second edge.

24. The method of claim 23, wherein the first edge is a rising edge, the second edge is a falling edge, and the third edge is a rising edge.

25. The method of claim 23, wherein the first edge is a falling edge, the second edge is a rising edge, and the third edge is a falling edge.

26. A sampling device, comprising:

a first delaying means and a second delaying means in a parallel configuration, the first delaying means and the second delaying means for receiving a clock signal and for generating one or more delayed signals based on the clock signal; and

controlling means responsive to an output of the first delaying means and the clock signal, the controlling means for

adjusting a delay amount of the first delaying means based on a difference between the output of the first delaying means and the clock signal, the controlling means further responsive to an output of the second delaying means, the controlling means further for adjusting a delay amount of the second delaying means based on a difference between the output of the second delaying means and the clock signal.

27. The device of claim 26, further including data sampling means, the data sampling means for sampling a data signal synchronized with the clock signal.

28. The device of claim 27, wherein the data sampling means is for sampling the data signal based on a sampling output of the first delaying means.

29. The device of claim 27, wherein the data sampling means is further for sampling the data signal based on a sampling output of the second delaying means.

30. The device of claim 26, wherein the first delaying means includes a first delay element responsive to the clock signal and a second delay element responsive to an output of the first delay element.

31. The device of claim 30, further including data sampling means for sampling a data signal based on a sampling output of the first delay element.

32. The device of claim 26, wherein the second delaying means includes a first inverting delay element responsive to the clock signal and a second inverting delay element responsive to an output of the first inverting delay element.

33. The device of claim 26, wherein the controlling means includes a comparing means responsive to the output of the first delaying means and responsive to the clock signal, and wherein the controlling means further includes a first delay controlling means responsive to an output of the comparing means, the first delay controlling means for adjusting the delay amount of the first delaying means based on the output of the comparing means.

34. The device of claim 33, wherein the comparing means comprises an inverting phase detection means.

35. The device of claim 34, wherein the inverting phase detection means comprises a phase difference detecting means and a sense amplifying means.

36. The device of claim 35, wherein the inverting phase detection means further comprises a latch.

37. The device of claim 34, wherein the inverting phase detection means comprises a flip flop.

38. The device of claim 33, wherein the controlling means further includes a different comparing means responsive to the output of the second delaying means and responsive to the clock signal, and wherein the controlling means further includes a second delay controlling means responsive to an output of the different comparing means, the second delay controlling means for adjusting the delay amount of the second delaying means based on the output of the different comparing means.

39. The device of claim 26, wherein the device is configured to sample a data signal synchronized with the clock signal according to a double data rate (DDR) protocol.